ABSTRACT OF THE DISCLOSURE

[0054] One embodiment of a distributed memory module cache includes tag memory and associated logic implemented at the memory controller end of a memory channel. The memory controller is coupled to at least one memory module by way of a point-to-point interface. The data cache and associated logic are located in one or more buffer components on each of the memory modules. Writes to a memory module are stored in the data cache which allows the writes to be postponed until the DRAM on the memory module is not busy.